AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application.

Listing of Claims:

1. (Currently Amended) A data processor comprising at least two processor cores, each said processor core having a first interface supporting a first bus coupled to an associated one of at least two program memories, a second interface supporting a second bus coupled to a common data memory accessible by each of said at least two processor cores, and a third interface supporting a third bus coupled to at least one input/output device accessible by each of said at least two processor cores, each of said first, second and third buses comprise an address bus that is sourced from one of said processor cores and a data bus, where said at least two processor cores are contained within a single integrated circuit package, and where said integrated circuit package is installed within a mobile station, where a first processor core functions as a CPU for controlling the overall operations of said mobile station, including a user interface, and where a second processor core functions as a DSP for controlling aspects of the wireless operation of said mobile station.

2. (Original) A data processor as in claim 1, wherein said first interface supports a unidirectional data bus, and wherein said second interface and said third interface each support a bidirectional data bus.

3. Cancelled

4. (Previously Presented) A data processor as in claim 1, wherein each of said at least two processor cores has said second interface coupled to said common data memory through a common memory control unit.

5. (Previously Presented) A data processor as in claim 1, wherein each of said at least two processor cores has said third interface coupled to at least one of a plurality of interface devices through a common control bus unit.

6. (Previously Presented) A data processor comprising at least one processor core, said processor core having a first interface supporting a first bus coupled to a program memory, a second interface supporting a second bus coupled to a data memory, and a third interface supporting a third bus coupled to at least one input/output device, each of said first, second and third buses comprise an address bus that is sourced from the processor core and a data bus, wherein said processor core operates with a clock signal, and fetches an instruction from said program memory using said address bus and said data bus of said first interface, the instruction fetch being referenced to a predetermined edge of said clock signal, said processor core beginning an execution of said fetched instruction on a next occurrence of said predetermined edge of said clock signal.

7. (Original) A data processor as in claim 6, wherein said first interface is responsive to an assertion of a HOLD signal for suspending the fetching of a next instruction from said program memory.

8. Cancelled

9. Cancelled

10. (Currently Amended) A mobile station as in claim ~~9~~ 13, wherein said first interface supports a unidirectional data bus, and wherein said second interface and said third interface each support a bidirectional data bus.

11. (Currently Amended) A mobile station as in claim ~~9~~ 13, wherein each of said plurality of processor cores has said second interface coupled to said common data memory through a

common memory control unit.

12. (Currently Amended) A mobile station as in claim ~~9~~ 13, wherein each of said plurality of processor cores has said third interface coupled to at least one of a plurality of interface devices through a common control bus unit.

13. (Previously Presented) A mobile station comprising an RF transceiver and a user interface, said mobile station further comprising a plurality of data processor cores, each of said data processor cores having a first interface supporting a first bus coupled to an associated one of a plurality of program memories, a second interface supporting a second bus coupled to a common data memory, and a third interface supporting a third bus coupled to at least one input/output device, each of said first, second and third buses comprise an address bus that is sourced from the processor core and a data bus, said plurality of data processor cores being contained within a single integrated circuit package, where a first processor core functions as a CPU for controlling the overall operation of said mobile station, including said user interface, and where a second processor core functions as a DSP for controlling operation of said RF transceiver, wherein each of said processor cores operates with a clock signal and fetches an instruction from said associated one of said plurality of program memories using said address bus and said data bus of said first interface, the instruction fetch being referenced to a predetermined edge of said clock signal, each said processor core beginning an execution of said fetched instruction on a next occurrence of said predetermined edge of said clock signal.

14. (Original) A mobile station as in claim 13, wherein said first interface is responsive to an assertion of a HOLD signal for suspending the fetching of a next instruction from said program memory.

15. (Previously Presented) A method for operating a data processor comprising providing at least one processor core, said processor core having a first interface supporting a program bus

coupled to a program memory, a second interface supporting a data bus coupled to a data memory, and a third interface supporting a control bus coupled to at least one interface device, each of said first, second and third buses comprise an address bus that is sourced from the processor core and a data bus, further comprising providing a clock signal and, in synchronism with a predetermined edge of said clock signal, fetching a program instruction from the program memory over a program bus, decoding a fetched instruction, beginning execution of the decoded instruction during a next occurrence of the predetermined edge of said clock signal and, depending on the decoded instruction, at least one of reading data from or writing data to the data memory over the data bus and reading data from or writing data to the interface device over the control bus.

16. (Original) A method as in claim 15, wherein each of said program, data and control buses comprise a data bus and an address bus that is sourced from said data processor.

17. (Original) A method as in claim 15, wherein said program bus supports a unidirectional data bus.

18. (Original) A method as in claim 15, and responsive to an assertion of a HOLD signal, suspending the fetching of a next instruction from said program memory.